CONVERTING STATE DIAGRAMS INTO SYNTHESIZEABLE VHDL

by

Thomas Clayton Mayo

A Thesis Submitted to the Graduate

Faculty of Rensselaer Polytechnic Institute
in Partial Fulfillment of the
Requirements for the Degree of
MASTER OF ENGINEERING

Approved:	
- I - I - D	
Dr. Kenneth Rose	
Thesis Adviser	

Rensselaer Polytechnic Institute Troy, New York August 1995